

CoreLink™ TLX-400 Network Interconnect Thin Links

Revision: r0p0

**Supplement to CoreLink NIC-400 Network Interconnect
Technical Reference Manual**



CoreLink TLX-400 Network Interconnect Thin Links

Supplement to CoreLink NIC-400 Network Interconnect Technical Reference Manual

Copyright © 2012 ARM. All rights reserved.

Release Information

The following changes have been made to this book.

Change history			
Date	Issue	Confidentiality	Change
02 July 2012	A	Non-Confidential	First issue for r0p0

Proprietary Notice

Words and logos marked with ® or ™ are registered trademarks or trademarks of ARM® in the EU and other countries, except as otherwise stated below in this proprietary notice. Other brands and names mentioned herein may be the trademarks of their respective owners.

Neither the whole nor any part of the information contained in, or the product described in, this document may be adapted or reproduced in any material form except with the prior written permission of the copyright holder.

The product described in this document is subject to continuous developments and improvements. All particulars of the product and its use contained in this document are given by ARM in good faith. However, all warranties implied or expressed, including but not limited to implied warranties of merchantability, or fitness for purpose, are excluded.

This document is intended only to assist the reader in the use of the product. ARM shall not be liable for any loss or damage arising from the use of any information in this document, or any error or omission in such information, or any incorrect use of the product.

Where the term ARM is used it means “ARM or any of its subsidiaries as appropriate”.

Confidentiality Status

This document is Non-Confidential. The right to use, copy and disclose this document may be subject to license restrictions in accordance with the terms of the agreement entered into by ARM and the party that ARM delivered this document to.

Product Status

The information in this document is final, that is for a developed product.

Web Address

<http://www.arm.com>

Contents

**CoreLink TLX-400 Network Interconnect Thin Links
Supplement to CoreLink NIC-400 Network
Interconnect Technical Reference Manual**

Chapter 1	Introduction	
	1.1 About the product	1-2
	1.2 Key features	1-3
	1.3 Product revisions	1-4
Chapter 2	Functional Description	
	2.1 Interfaces	2-2
	2.2 Operation	2-5
Appendix A	Revisions	

Chapter 1

Introduction

This chapter introduces the CoreLink™ TLX-400 Network Interconnect Thin Links. It contains the following sections:

- *About the product* on page 1-2
- *Key features* on page 1-3
- *Product revisions* on page 1-4.

1.1 About the product

The CoreLink TLX-400 Network Interconnect Thin Links is an extension to the CoreLink NIC-400 Network Interconnect base product and provides a mechanism to reduce the number of signals in an AXI point-to-point connection and enable it to be routed over a longer distance.

1.2 Key features

The CoreLink TLX-400 Network Interconnect Thin Links has the following features:

- Thin Links reduce routing congestion and aids timing closure of point to point connections.
 - Point to point connections are implemented as forward and reverse links. Each link can be independently configured to reduce the number of wires the connection requires.
- To aid physical implementation Thin Links supports clock domain crossing.
 - The end points of a Thin Link are always specified as different clocks. The relationship of the clocks must be defined as asynchronous.
- Thin Links can incorporate other NIC-400 functions. For example:
 - a connection between components of different data widths
 - a connection between components of different protocols.
- You can use Thin Links in conjunction with *Quality of Service for Virtual Networks (QVN-400)*. For more information, see the *CoreLink QVN-400 Network Interconnect Advanced Quality of Service for Virtual Networks, Supplement to CoreLink NIC-400 Network Interconnect Technical Reference Manual*.
- You can use Thin Links in conjunction with *Advanced Quality of service (QoS-400)*. For more information, see the *CoreLink QoS-400 Network Interconnect Advanced Quality of Service, Supplement to CoreLink NIC-400 Network Interconnect Technical Reference Manual*.
- A Thin Link implementation is partitioned into two layers:
 - *Data Link Layer (DLL)*
 - *Physical Layer (PL)*.
- The DLL performs:
 - channel identification of transfer packets across the link
 - buffering of transfer packets at the destination end of the link
 - arbitration between transfer packets on to the link
 - packing of transfer packet on to the link
 - flow control across the link.
- You can modify or replace the PL to enable different physical implementations.
- You can enable hierarchical clock gating support for the destination domain.
- You can configure support for power domain crossing.

1.3 Product revisions

This section describes the differences in functionality between product revisions:

r0p0 First release.

Chapter 2

Functional Description

This chapter provides a functional description of the CoreLink TLX-400 Network Interconnect Thin Links and how it works. It contains the following sections:

- [Interfaces on page 2-2](#)
- [Operation on page 2-5.](#)

2.1 Interfaces

TLX-400 enables TLX protocol functionality to be added to NIC-400 slave and master interfaces in a larger system, as shown in [Figure 2-1](#).

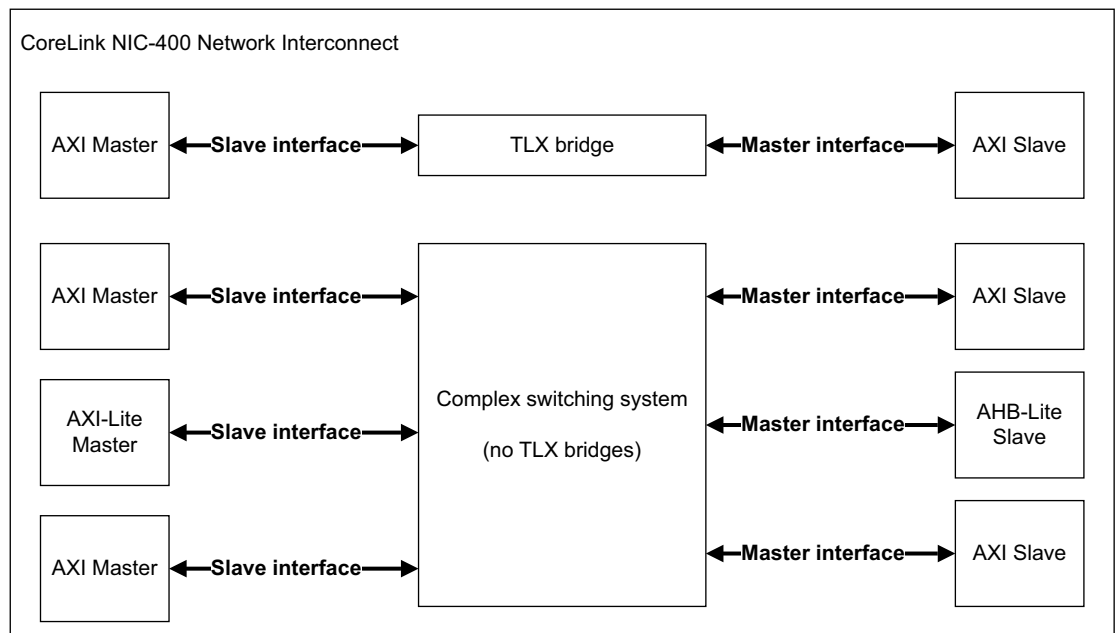


Figure 2-1 TLX configured in a larger system

2.1.1 Slave interfaces

Within NIC-400, you can only configure TLX as a bridge, that is, a TLX can only support a single slave interface. However, it is possible for a TLX bridge to be configured within a larger NIC, as shown in [Figure 2-1](#).

The TLX supports all the slave interfaces that the base NIC-400 product does, those are:

- AXI3
- AXI4
- AHB-Lite slave
- AHB-Lite mirrored master.

You can only configure an AHB slave interface if the master interface is not of type AHB, that is, neither an AHB to AHB bridge or an AHB to AHB thin link bridge are supported.

You can configure a slave interface to support QVN if:

- the QVN product license is installed
- the slave interface type is AXI3 or AXI4.

See the *CoreLink QVN-400 Network Interconnect Advanced Quality of Service for Virtual Networks Supplement to CoreLink NIC-400 Network Interconnect Technical Reference Manual*.

2.1.2 Master interfaces

Within NIC-400, you can only configure TLX as a bridge, that is, a TLX can only support one master interface. However, it is possible for a TLX bridge to be configured within a larger NIC, as shown [Figure 2-1](#).

The TLX supports all the master interfaces that the base NIC-400 product does, those are:

- AXI3
- AXI4
- AHB-Lite slave
- AHB-Lite mirrored master.

You can only configure an AHB master interface provided the slave interface is not type AHB, that is, neither an AHB to AHB bridge or an AHB to AHB thin link bridge are supported.

You can configure a master interface to support QVN if:

- the QVN product license is installed
- the slave interface type is AXI3 or AXI4
- the slave interface is configured to support QVN.

See the *CoreLink QVN-400 Network Interconnect Advanced Quality of Service for Virtual Networks Supplement to CoreLink NIC-400 Network Interconnect Technical Reference Manual*.

2.1.3 Low power interface

This section describes:

- [Hierarchical clock gating interfaces](#)
- [Power domain crossing interfaces](#).

Hierarchical clock gating interfaces

When a TLX bridge is configured to support hierarchical clock gating there is a *Low Power Interface* (LPI) to enable that output from the master interface clock domain, see *AMBA Specification* for more information.

When the LPI indicates that the low power state has been entered then the clock for the master interface domain can be clock gated.

Power domain crossing interfaces

When a bridge is configured to support *Power Domain Crossing* (PDC), hierarchical clock gating support is also included.

An additional PDC LPI is output from the slave domain to support the power gating sequence. When the PDC LPI is changing its mode of operation, the slave domain clock is required to be operational. This is indicated by the bridge slave domain by asserting an additional LPI **CACTIVE** signal.

If the PDC LPI indicates that the low power state has been entered, either power domain can be power gated.

Note

- If the master domain is powered down, any transactions issued to the slave domain will be stalled at the interface.
- The PDC LPI indicates this condition by asserting its PDC **CACTIVE** signal.

2.1.4 Physical layer interfaces

You can replace the physical layer to enable flexibility in the implementation.

There are two interfaces in each direction. These are AXI stream compliant, see *AMBA Specification* for more information.

Forward direction

These interfaces consist of:

AXI stream data interface

AXI stream data interface. This has the data width defined by the forward link width from the GUI.

AXI stream flow control interface

This has the data width of the number of downstream channels which are R and B for an AXI to AXI bridge.

Reverse direction

These interfaces consist of:

AXI stream data interface

This has the data width defined by the reverse link width from the GUI.

AXI stream flow control interface

AXI stream flow control interface. This has the data width of the number of upstream channels that is, AW, AR and W multiplied by the number of virtual networks if QVN is enabled.

2.2 Operation

Figure 2-2 shows the Thin Links hierarchy:

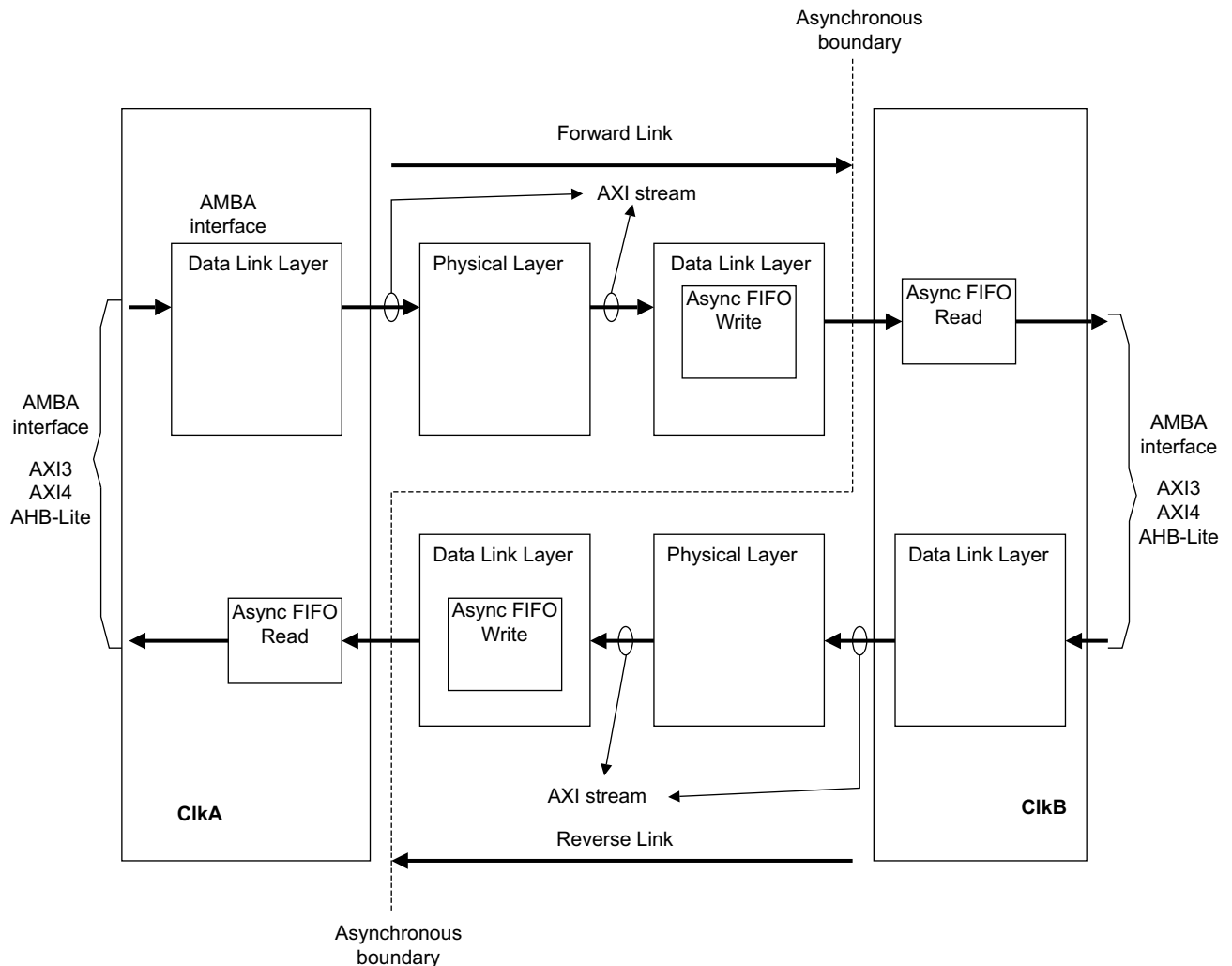


Figure 2-2 Thin Links hierarchy

2.2.1 Thin Link

The thin link consists of two AXI stream interfaces for each direction.

- Forward data
- Reverse data
- Forward flow
- Reverse flow.

The data stream links are used to transport the AMBA forward and reverse channel beats. The flow stream interfaces are used for replenishment of credit tokens.

This architecture means that the thin link bridge operation is independent of the physical layer latency.

This section describes:

- [Forward AMBA channels on page 2-6](#)
- [Reverse AMBA channels on page 2-6](#)

- [Data packing](#)
- [Arbitration on page 2-7.](#)

Forward AMBA channels

To guarantee that the data link does not stall and therefore cause blocking between channels, a forward channel beat is only issued onto the forward data stream link when that channel has credit, indicating that there is space at the destination to accept that beat. So a channels credit is consumed when a beat is issued into the physical layer data stream link. The number of credits is equal to the number of buffer slots available for that channel at the destination. When the credits are all consumed for a channel, then no more beats are issued onto the data stream interface.

When a destination buffer slot is emptied by that beat being issued downstream out of the thin link bridge then a flow control credit for that channel is returned back across the reverse flow control stream link.

Reverse AMBA channels

To guarantee that the data link does not stall and therefore cause blocking between channels, a reverse channel beat is issued onto the reverse data stream link when that channel has credit, indicating that there is space at the destination to accept that beat. So a channels credit is consumed when a beat is issued into the physical layer data stream link. The number of credits is equal to the number of buffer slots available for that channel at the destination. When the credits are all consumed for a channel then no more beats are issued onto the data stream interface.

When a destination buffer slot is emptied by that beat being issued back upstream out of the thin link bridge, then a flow control credit for that channel is returned back across the forward flow control stream link.

Data packing

There are five different packing strategies:

- Widest Width
- Widest Width / 2
- Widest Width / 4
- Address Width + Data Width or Response + Read Data Width
- User Defined.

Note

There is no requirement to have the same data packing in forward and reverse directions.

Widest Width

This is the width of the widest channel in a forward or reverse direction.

Widest Width / 2

This is half the width of the widest channel in a forward or reverse direction.

Widest Width / 4

This is quarter of the width of the widest channel in a forward or reverse direction.

Address Width + Data Width or Response + Read Data Width

This is the widest address channel plus the widest data width in the forward or the width of the read data plus response in the reverse link.

User Defined (in Bytes)

This is any multiple byte width up to a maximum of the widest channel divided by 2.

Note

See also *Configuring Thin Links* in the *Configuring the Network* chapter of the *CoreLink NIC-400 Network Interconnect Supplement to CoreLink ADR-400 AMBA Designer User Guide*.

Arbitration

This entails arbitration of which channel to issue to the link. When there is a choice, it is achieved by using the **AWQOS** value, **ARQOS** value or the W channel associated with the **AWQOS** value. The reverse link selection uses a round robin arbitration.

Note

For more information on **AxQOS** values, see the *CoreLink QoS-400 Network Interconnect Advanced Quality of Service, Supplement to CoreLink NIC-400 Network Interconnect Technical Reference Manual*.

Appendix A

Revisions

This appendix describes the technical changes between released issues of this book.

Table A-1 Issue A

Change	Location	Affects
First release	-	-